CLAIMS

1. An integrated circuit, comprising a processor, an onboard system clock for generating a clock signal, and clock trim circuitry, the integrated circuit being configured to:

(a) receive an external signal;

(b) determine either the number of cycles of the clock signal during a predetermined number of cycles of the external signal, or the number of cycles of the external signal during a predetermined number of cycles of the clock signal;

(c) store a trim value in the integrated circuit, the trim value having been determined on the basis of the determined number of cycles; and

(d) use the trim value to control the internal clock frequency.

2. An integrated circuit according claim 1, the integrated circuit being configured to, between steps (b) and (c):

output the result of the determination of step (b); and

receive the trim value from an external source.

3. An integrated circuit according to claim 1, wherein the integrated circuit includes non-volatile memory, and (c) includes storing the trim value in the memory.

4. An integrated circuit according to claim 3, where the memory is flash RAM.

5. An integrated circuit according to claim 3, wherein step (d) includes loading the trim value from the memory into a register and using the trim value in the register to control a frequency of the internal clock.

6. An integrated circuit according to claim 1, wherein the trim value is determined and stored permanently in the integrated circuit.

7. An integrated circuit according to claim 6, wherein the circuit includes one or more fuses that are intentionally blown following step (c), thereby preventing the stored trim value from subsequently being changed.

8. An integrated circuit according to claim 1, wherein the system clock further includes a voltage controlled oscillator (VCO), an output frequency of which is controlled by the trim value.

9. An integrated circuit according to claim 8, further including a digital to analog convertor configured to convert the trim value to a voltage and supply the voltage to an input of the VCO, thereby to control the output frequency of the VCO.

10. An integrated circuit according to claim 1, wherein the integrated circuit is configured to operate under conditions in which the signal for which the number of cycles is being determined is at a considerably higher frequency than the other signal.

11. An integrated circuit according to claim 10, configured to operate when a ratio of the number of cycles determined in step (b) and the predetermined number of cycles is greater than about 2.

12. An integrated circuit according to claim 11, wherein the ratio is greater than about 4.

13. An integrated circuit according to claim 1, disposed in a package having an external pin for receiving the external signal.

14. An integrated circuit according to claim 13, wherein the pin is a serial communication pin configurable for serial communication when the trim value is not being set.

15. An integrated circuit according to claim 1, wherein the trim value was also determined on the basis of a compensation factor that took into account a temperature of the integrated circuit when the number of cycles are being determined.

16. An integrated circuit according to claim 2, wherein the trim value received was determined by the external source, the external source having determined the trim value including a compensation factor based on a temperature of the integrated circuit when the number of cycles are being determined.

17. An integrated circuit according to claim 1, wherein the trim value is determined by performing a number of iterations of determining the number of cycles, and averaging the determined number.